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REMARKS

Applicant appreciates the courtesy extended by Examiner Pan in conducting a telephone interview with Applicant's representative on September 7, 2006. During the telephone interview, Applicant's representative described the Applicant's claimed invention and distinguished the claimed invention from the prior art. The Examiner indicated that further consideration was needed before allowing the claims.

Claims 13, 14, 17, 18, 20, and 26-30 are pending in the application. Claim 13 has been amended to incorporate the subject matter of claim 25, which has been canceled without prejudice. Claim 13 also has been amended to delete the language "operable" and "is designed" as noted on page 2 of the Office Action. As amended, independent claim 13 now incorporates the subject matter indicated as being allowable in the Office Action of 12/21/2005.

Applicant's claimed invention recites a processor system with an instruction executing means including at least a first executing unit connected to a first databus, and a second executing unit connected to a second databus, the first databus having a lower transmission rate than the second databus (see claim 13).

As recited in claim 13, the first executing unit is designed to execute **all types** of instructions of the processor system, while the second executing unit is designed to execute **only a few special** instructions.

Further, claim 13 recites that a path leading to the first executing unit is temporarily deactivated if no instruction has to be executed by the first executing unit (see claim 13, last paragraph; and specification at page 8, lines 10-15).

Claims 13, 14, and 30 were rejected under 35 USC §103(a) as being unpatentable over U.S. Patent 5,559,986 to Alpert et al. ("Alpert") in view of U.S. Patent 5,634,131 to Matter et al. ("Matter"). Claim 20 was rejected under 35 USC §103(a) as being unpatentable over Alpert in view of Matter, and further in view of U.S. Patent 5,841,771 to Irwin et al. ("Irwin"). Claims 17 and 18 were rejected under 35 USC §103(a) as being unpatentable over Alpert in view of Matter,

and further in view of U.S. Patent 4,196,470 to Berg. Claims 25-29 were rejected under 35 USC §103(a) as being unpatentable over Alpert in view of Matter, and further in view of Irwin. These rejections are respectfully traversed.

As amended, independent claim 13 incorporates the subject matter of claim 25. Therefore, the rejections of claims 13 and 25 will now be addressed.

On page 3, paragraph #6 of the Office Action of 07/14/2006, it was admitted that Alpert does not teach or suggest temporarily "deactivat[ing] the first executing unit if momentarily no instruction to be executed."

The Matter reference was cited allegedly to remedy this deficiency of Alpert. Referring to FIG. 3 of Matter, clock signals of a floating point unit 202 are disabled "when floating point unit 202 is not currently executing an instruction and is not preparing to execute an instruction" (see column 7, lines 21-28 of Matter). As stated in Matter: "Thus, the clock of floating point unit 202 will automatically be stopped if there is no new floating point instruction prepared for execution and when any current floating point instruction has completed execution" (column 7, lines 32-36).

However, Matter does not teach or suggest a processor system having a plurality of executing units for parallel execution of instructions, the executing units connected to databuses with different transmission rates, as recited in claim 13. Therefore, even if Matter was somehow combined with Alpert, there would be no teaching or suggestion of a processor unit for parallel execution of instructions, including first and second executing units connected to respective databuses where the first executing unit is temporarily deactivated, while still enabling execution of instructions by the second executing unit.

Regarding the rejection of claim 25, on page 6, paragraph #16 of the Office Action of 07/14/2006, it was admitted that Alpert does not teach or suggest a first databus having a lower transmission rate than a second databus.

The Irwin reference was cited allegedly to remedy this deficiency of Alpert. However, the Irwin reference was already addressed in the response filed on April 6, 2005, which arguments are incorporated by reference herein. In particular, Irwin does not teach or suggest a plurality of executing units for parallel execution of instructions. Irwin merely discloses a plurality of **latches**, which are not equivalent to executing units for executing instructions in parallel, as recited in claim 13.

Irwin also does not teach or suggest a plurality of databuses connected to a plurality of executing units. Instead, Irwin discloses databuses for header octets (i.e., the receive header bus 544) or for payload octets (i.e., the receive TDM bus A 546).

Since Irwin does not teach or suggest databuses corresponding to a plurality of executing units (but instead discloses **latches**, and databuses for header octets) or two databuses having different transmission rates, it cannot be combined with the microprocessor taught by Alpert to somehow produce the Applicant's claimed invention.

For at least the reasons discussed above, the proposed combination of Alpert in view of Matter, and further in view of Irwin does not teach or suggest the Applicant's claimed invention. Therefore, independent claim 13 and its dependent claims are patentable over the proposed combination.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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